

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-051020

(43)Date of publication of application : 18.02.1997

(51)Int.CI.

H01L 21/60
G06K 19/077

(21)Application number : 07-201986

(71)Applicant : HITACHI LTD

(22)Date of filing : 08.08.1995

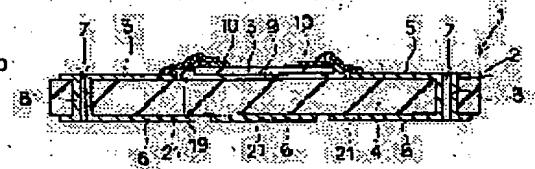
(72)Inventor : ENDO TSUNEO

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD AND IC CARD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can be thinner.

SOLUTION: A semiconductor device having a wiring board 4 on the rear face of which an external terminal 21 is provided, a semiconductor chip 3 fixed to the principal face of the wiring board, and connection means electrically connecting electrodes 10 to wirings 5 and 6 of the wiring board 4, respectively, comprises an insulator coating at least a conductive part extending from the periphery of the semiconductor chip 3 to the end face, and a conductive layer electrically connecting the electrodes 10 to the wirings of the wiring board. The thickness of the semiconductor chip is about 5-30 μ m.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device which is a semiconductor device which has the connecting means which connects electrically the wiring substrate which has an external terminal at the rear face, the semiconductor chip fixed to the principal plane of said wiring substrate, and the electrode of said semiconductor chip and wiring of a wiring substrate, and is characterized by to have the conductor layer which connects electrically a wrap insulator, the electrode of said semiconductor chip, and wiring of a wiring substrate for the conductive part which attains to an end face from the periphery of said semiconductor chip at least.

[Claim 2] Said semiconductor chip is a semiconductor device according to claim 1 characterized by having thickness around 5-30 micrometers.

[Claim 3] Said wiring substrate, an insulator, and a conductor layer are a semiconductor device according to claim 1 characterized by being formed with the heat-resistant ingredient.

[Claim 4] Said wiring substrate, an insulator, and a conductor layer are a semiconductor device according to claim 1 characterized by being formed with the resin system ingredient which has flexibility.

[Claim 5] The wiring substrate which has an external terminal at the rear face, and the semiconductor chip fixed to the principal plane of said wiring substrate, The process which is the manufacture approach of a semiconductor device of having the connecting means which connects electrically the electrode of said semiconductor chip, and wiring of a wiring substrate, removes the rear face of a semiconductor chip and is formed in the thickness around 5-30 micrometers, The process which fixes a semiconductor chip to the principal plane of said wiring substrate through an insulating glue line, The manufacture approach of the semiconductor device characterized by having the process which connects electrically the electrode of said semiconductor chip, and wiring of a wiring substrate with a wrap process for the conductive part ranging from the edge to an end face of said semiconductor chip to expose by print processes with an insulator at a conductor layer.

[Claim 6] The manufacture approach of the semiconductor device according to claim 5 characterized by pressing down a semiconductor chip and making said insulating glue line protrude from the edge of a semiconductor chip outside while laying a semiconductor chip on said insulating glue line after printing an insulating glue line to a wiring substrate, in case a semiconductor chip is fixed to said wiring substrate through an insulating glue line.

[Claim 7] The wiring substrate with which it is the IC card which comes to incorporate the semiconductor device which has the external terminal exposed to the hollow of a card base material through adhesives, and said semiconductor device has an external terminal at the rear face, While consisting of a semiconductor device which has the connecting means which connects electrically the semiconductor chip fixed to the principal plane of said wiring substrate, and the electrode of said semiconductor chip and wiring of a wiring substrate It is the IC card characterized by having the conductor layer which connects electrically a wrap insulator, the electrode of said semiconductor chip, and wiring of a wiring substrate for the conductive part which attains to an end face from the periphery of said semiconductor chip at least, and said semiconductor chip serving as thickness of dozens of micrometers.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] About a semiconductor device, its manufacture approach, and an IC card, especially this invention is applied to manufacture of a thin semiconductor device, and relates to an effective technique.

[0002]

[Description of the Prior Art] As one structure of an IC card, HAME **** structure is known by the card with a thickness of 0.76mm in the module which transfer-molded the LSI chip as indicated by the Nikkei Business Publications issue "Nikkei micro device" March, 1988 issue, March [of the same year] 1 issue, and P56-P62. Said module (semiconductor device) is a semiconductor chip while connecting the electrode of a semiconductor chip, and wiring of a wiring substrate electrically by wirebonding, after mounting a semiconductor chip in the whole surface of the wiring substrate which consists of a glass-epoxy resin by COB (chip on board). It is manufactured by transfer-molding a wire etc. Moreover, the contact electrode terminal used as an external terminal is prepared in the rear face of said wiring substrate. This contact electrode terminal is electrically connected to wiring of the principal plane of a wiring substrate by the conductor with which the through hole established in said wiring substrate was filled up.

[0003] PWC for IC cards (Printed Wiring Connection) which, on the other hand, used the conductive paste for connection instead of the bonding wire in order to attain productivity and densification to issue, P26-P27, and P38-P39 on Kogyo Chosakai Publishing issue "newest hybrid-packaging technical" May 15, 1988 — yes, Brit's IC example is indicated.

[0004] After the assembly by former PWC inserts an LSI chip in the part which carried out opening to the polycarbonate sheet, it is embedded, and it covers a vertical side with a polycarbonate film while it covers the front face of a polycarbonate sheet, and the embedding part on an LSI chip and forms printing connection wiring by printing after that.

[0005] Moreover, in the case of the latter hybrid IC, IC chip is embedded with an epoxy resin in aluminum substrate, and it has structure which wired using photosensitive conductive paste and an insulating paste.

[0006] In addition, with such structures, while becoming the structure which embeds a semiconductor chip at a wiring substrate, the front face of a wiring substrate and the electrode formed on the semiconductor chip have structure on an abbreviation same flat surface. Therefore, it is in the condition that a level difference does not occur between the electrode of a semiconductor chip, and wiring of a wiring substrate, on the occasion of formation of the conductive pattern for connection (conductor layer).

[0007]

[Problem(s) to be Solved by the Invention] With the semiconductor device (module) of COB structure, since the electrode of a semiconductor chip and wiring of a wiring substrate serve as structure connected by wirebonding, only in a part, a semiconductor device becomes thick in wire loop-formation height, with HAME **** (it embeds) structure, the hollow of a HAME **** sake becomes deep and the mechanical strength of the hollow part of an IC card becomes low at an IC card.

[0008] With the structure which embeds a semiconductor chip on the other hand at a part for the hole

prepared in the wiring substrate, as it became the same field about the front face of wiring of a wiring substrate, and the electrode of a semiconductor chip, the level difference was lost, and the approach of connecting the electrode of a semiconductor chip and wiring electrically by print processes is adopted. However, it is difficult for there to be problems, like exchange (repair) is very difficult, when the embedding of a semiconductor chip taking time and effort and a defective are generated, and to make cheaply. In order to make cheaply, it is required to carry a semiconductor chip directly on a wiring substrate.

[0009] Since a conductor layer does not become high, the structure of connecting wiring with the electrode of a semiconductor chip by the conductor layer by print processes can attain thin shape-ization of a semiconductor device (module).

[0010] Then, this invention considered connecting the electrode of a semiconductor chip, and wiring by print processes while carrying the semiconductor chip in the principal plane of a wiring substrate. However, when a level difference arose between the electrode of a semiconductor chip, and wiring since the thickness is set to 200 micrometers – 500 micrometers, and the conventional semiconductor chip, i.e., an LSI chip, printed a conductive paste, it turned out that it is easy to generate a printing blur in said level difference section, and connecting becomes inadequate.

[0011] The purpose of this invention is to offer the semiconductor device which can attain thin shape-ization, and its manufacture approach.

[0012] Other purposes of this invention are to offer the IC card which can attain the improvement in a mechanical strength of a card base material.

[0013] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.

[0014]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is explained among invention indicated in this application. That is, the semiconductor device of this invention is a semiconductor device which has the connecting means which connects electrically the wiring substrate which has an external terminal at the rear face, the semiconductor chip fixed to the principal plane of said wiring substrate, and the electrode of said semiconductor chip and wiring of a wiring substrate, and has the structure have the conductor layer which connects electrically a wrap insulator, the electrode of said semiconductor chip, and wiring of a wiring substrate for the conductive part which attains to an end face from the periphery of said semiconductor chip at least. Said semiconductor chip serves as thickness around 5–30 micrometers. Moreover, said wiring substrate, the insulator, and the conductor layer are formed with the resin system ingredient which has flexibility while they are formed with the heat-resistant ingredient.

[0015] The wiring substrate with which the manufacture approach of the semiconductor device of this invention has an external terminal at the rear face, It is the manufacture approach of a semiconductor device of having the connecting means which connects electrically the semiconductor chip fixed to the principal plane of said wiring substrate, and the electrode of said semiconductor chip and wiring of a wiring substrate. The process which removes the rear face of a semiconductor chip and is formed in the thickness around 5–30 micrometers, The process which fixes a semiconductor chip to the principal plane of said wiring substrate through an insulating glue line, The conductive part ranging from the edge to an end face of said semiconductor chip to expose is consisted of a wrap process and a process which connects electrically the electrode of said semiconductor chip, and wiring of a wiring substrate by the conductor layer by print processes with the insulator. Moreover, in case a semiconductor chip is fixed to said wiring substrate through an insulating glue line, after printing an insulating glue line to a wiring substrate, while laying a semiconductor chip on said insulating glue line, press down a semiconductor chip and said insulating glue line is made to overflow the edge of a semiconductor chip outside, and a conductor layer is printed after that.

[0016] The wiring substrate with which the IC card of this invention is an IC card which comes to incorporate the semiconductor device which has the external terminal exposed to the hollow of a card base material through adhesives, and said semiconductor device has an external terminal at the rear

face, While consisting of a semiconductor device which has the connecting means which connects electrically the semiconductor chip fixed to the principal plane of said wiring substrate, and the electrode of said semiconductor chip and wiring of a wiring substrate Having [and] the conductor layer which connects electrically a wrap insulator, the electrode of said semiconductor chip, and wiring of a wiring substrate for the conductive part which attains to an end face from the periphery of said semiconductor chip at least, said semiconductor chip serves as thickness around 5-30 micrometers.

[0017]

[Function] According to the above mentioned means, since the electrode of a semiconductor chip and wiring of a wiring substrate are electrically connected by the conductor layer by printing while carrying the semiconductor chip which became thin with dozens of micrometers in a wiring substrate, the semiconductor device of this invention can attain thin shape-ization of a semiconductor device.

[0018] Since the conductive part by which an end face exposes the semiconductor device of this invention to the bottom of this conductor layer from the periphery of said semiconductor chip although the electrode of a semiconductor chip and wiring of a wiring substrate are electrically connected by the conductor layer by printing is prepared in the wrap insulator, the short circuit between the ***** electrode sections of a semiconductor chip does not occur.

[0019] The semiconductor device of this invention becomes good [the conductor layer / the thermal resistance of a semiconductor device], since the wiring substrate, the insulator, and the conductor layer are formed with the heat-resistant ingredient.

[0020] Since the semiconductor device of this invention is formed with the resin system ingredient with which a wiring substrate, an insulator, and a conductor layer have flexibility, the dependability of the electrical installation of the electrode of a semiconductor chip and wiring becomes high.

[0021] According to the manufacture approach of the semiconductor device of this invention, a thin semiconductor device can be manufactured from mounting in a wiring substrate, after making a semiconductor chip thin, and connecting the electrode of a semiconductor chip, and wiring of a wiring substrate by the conductor layer by print processes.

[0022] Since the periphery of a semiconductor chip and the conductive part of an end face are covered with an insulator, the short circuit between the ***** electrode sections of a semiconductor chip stops moreover, according to the manufacture approach of the semiconductor device of this invention, generating them, before connecting the electrode of a semiconductor chip, and wiring of a wiring substrate electrically by print processes.

[0023] Moreover, while laying a semiconductor chip on said insulating glue line, a semiconductor chip is pressed down and said insulating glue line is made to protrude from the edge of a semiconductor chip outside, after printing an insulating glue line to a wiring substrate, in case a semiconductor chip is fixed to said wiring substrate. Therefore, in printing of a subsequent conductor layer, since an insulating glue line extends between a semiconductor chip and wiring, the level difference between a semiconductor chip and a wiring substrate is reduced, and the electrical installation which the blur of the conductor layer which connects wiring with the electrode of a semiconductor chip etc. stops having occurred, and was stabilized becomes possible.

[0024] Since HAME ** rare ***** is thin-shape-ized, the IC card of this invention can make a semiconductor device shallow, and its mechanical strength of a card base material improves a HAME **** hollow in it.

[0025]

[Example] With reference to a drawing, one example of this invention is explained below. Drawing 1 is the typical sectional view showing the outline of the semiconductor device by one example of this invention. The typical sectional view and drawing 6 which show the condition that the typical sectional view and drawing 5 which shows the condition that the mimetic diagram in which drawing 2 - drawing 6 are drawings showing the important section of the semiconductor device in each process in the manufacture approach of the semiconductor device of this example, and drawing 2 shows a junction stratification condition, the typical sectional view in which drawing 3 shows the loading condition of a semiconductor chip, and drawing 4 formed the insulator formed the conductor layer are the typical top view showing

the condition formed the insulator and the conductor layer. The typical sectional view and drawing 8 which show the important section of the IC card according [drawing 7] to this example are the top view showing an IC card similarly.

[0026] The semiconductor device (module) 1 of this example has the structure of having the wiring substrate 2 and the semiconductor chip 3 carried in the principal plane of this wiring substrate 2, as it is a module for HAME ** rare ** IC cards and is shown in IC card 20 shown in drawing 7 and drawing 8 at drawing 1.

[0027] The wiring substrate 2 is the printed circuit board which consists of the substrate body 4, wiring 5 and 6 prepared in the principal plane (front face) and rear face of this substrate body 4, and a through hole 7 which penetrates said substrate body 4. Said substrate body 4 is a glass fiber from the so-called GARAEP0 substrate into which epoxy resin was infiltrated, and the ingredient of high thermal resistance into which BT resin was infiltrated. This substrate body 4 has thermal resistance also in 80 degrees C or more. Moreover, said substrate body 4 has become about 0.3mm in thickness. Said wiring 5 and 6 is formed by having pasted the front rear face of said substrate body 4, for example, etching copper foil with a thickness of about 35 micrometers into a desired pattern. Moreover, although illustration is not carried out to the front face of these wiring 5 and 6 so that connection by printing mentioned later may be made proper, partially or on the whole, plating processing by nickel and Au is performed.

[0028] Moreover, said through hole 7 is formed by carrying out drilling so that the substrate body 4 may be penetrated. Coppering is performed to the internal surface of this through hole 7. The predetermined wiring 5 and 6 on the rear face of front of the substrate body 4 is electrically connected by the conductor 8 formed of this coppering.

[0029] The wiring 6 of the rear face of the semiconductor device 1 of this example constitutes the contact electrode terminal 21 used as the external terminal of IC card 20, as shown in drawing 8.

[0030] Moreover, the semiconductor chip 3 is being fixed to the principal plane of the wiring substrate 2 through the insulating glue line 9. The rear-face side in which an active field is not established is removed by etching etc. in fixed thickness, for example, the semiconductor chip 3 serves as thickness of about 5-30 micrometers. This is for making it the level difference of the electrode 10 prepared in the front face of a semiconductor chip 3 and the height of the wiring 5 of the wiring substrate 2 not become large.

[0031] Moreover, as shown in drawing 6 , the insulator 11 formed with the ingredient which has flexibility and has thermal resistance is formed so that the conductive part of said semiconductor chip 3 which attains to an end face from a periphery may be covered at least. Said insulator 11 is formed with the resin system ingredient which has thermal resistance above 80 degrees C. Moreover, the conductor layer 12 formed with the ingredient which has flexibility on said insulator 11, and has thermal resistance is formed. A conductor layer 12 connects electrically the electrode 10 of said semiconductor chip 3, and the wiring 5 of the wiring substrate 2. Said conductor layer 12 is formed with the resin system ingredient which has thermal resistance above 80 degrees C. Said insulator 11 and conductor layer 12 are formed by screen printing.

[0032] In addition, from the edge of a semiconductor chip 3, since the insulating glue line 9 which connects a semiconductor chip 3 to the substrate body 4 overflows and a part exists, in order that [said] it may overflow and a part may mitigate the level difference between a semiconductor chip 3 and the substrate body 4, flattening of the insulator 11 formed in the part covering the edge of wiring 5 is carried out to the perimeter of said semiconductor chip 3, and it is formed in it. Flattening also of the conductor layer 12 prepared on this insulator 11 by which flattening was carried out is carried out, and the blur [like] which becomes inconvenient to electrical installation, such as becoming thin partially, stops therefore, producing it.

[0033] Moreover, as shown in drawing 6 , since a conductor layer 12 is formed on said insulator 11 while said insulator 11 is continued and formed in a part for the point of wiring 5 from the edge of a semiconductor chip 3, the short circuit between the adjoining electrodes 10 is prevented.

[0034] Since the semiconductor device 1 of this example is formed so that the conductor layer 12 to which a semiconductor chip 3 connects being thinly formed with 5-30 micrometers, and the electrode

10 of a semiconductor chip 3 and the wiring 5 of the wiring substrate 2 may crawl on the wiring substrate 2 top through an insulator 11, it becomes thin sharply as compared with wirebonding structure. That is, while a semiconductor chip with a thickness of 200–500 micrometers is laid on the wiring substrate 2 in the case of the conventional wirebonding structure, the wire with which wire loop-formation height is set to about 150 micrometers is connected to the electrode of this semiconductor chip. Moreover, said wire and semiconductor chip are covered with the package formed of transfermold. Therefore, the height from the front face of a wiring substrate to a package top face becomes high with about at least 500 micrometers. On the other hand, since neither a semiconductor chip nor a conductor layer is covered with a package in the case of the semiconductor device of this example, single or more figures become low with about 15–40 micrometers, and the height from the front face of a wiring substrate to the top face of a conductor layer can attain thin shape-ization of a semiconductor device 1. For this reason, as shown in drawing 7, the mechanical strength of card base material which was formed in card base material 23 and with which about 10 micrometers of said hollows 25 can be conventionally made shallow more than 100 HAME **** case by becoming depressed 25, and hollow 25 is formed 23 part improves the semiconductor device 1 of this example through the insulating adhesives 24.

[0035] The semiconductor device of this example does the following effectiveness so.

[0036] (1) Since the semiconductor device of this example serves as the structure of carrying the semiconductor chip of the thickness around 5–30 micrometers in the principal plane of a substrate body, thin shape-ization of a semiconductor device is attained.

[0037] (2) Since the semiconductor device of this example is connected by the conductor layer in which the connection between the electrode of a semiconductor chip and wiring of a wiring substrate is formed of print processes, thin shape-ization of a semiconductor device is attained.

[0038] (3) In the semiconductor device of this example, since the insulator and wiring substrate used as the substrate of the conductor layer which connects the electrode of a semiconductor chip and wiring of a wiring substrate, and a conductor layer are formed with the resin system ingredient which has flexibility, the dependability of the electrical installation of the electrode of a semiconductor chip and wiring of a wiring substrate becomes high.

[0039] (4) In the semiconductor device of this example, since the insulator and wiring substrate used as the substrate of the conductor layer which connects the electrode of a semiconductor chip and wiring of a wiring substrate, and a conductor layer are formed with the heat-resistant ingredient, its thermal resistance of a semiconductor device improves.

[0040] (5) Since the insulator is formed in the bottom of the conductor layer which connects the electrode of a semiconductor chip, and wiring of a wiring substrate, the short circuit prevention effectiveness between conductor layers becomes high, and the inter-electrode short circuit of a semiconductor device stops occurring in the semiconductor device of this example.

[0041] Below, drawing 2 – drawing 6 are used and explained about the manufacture approach of the semiconductor device 1 of this example. As shown in drawing 2, the wiring substrate 2 is prepared first. This wiring substrate 2 is the printed circuit board which consists of the substrate body 4, wiring 5 and 6 prepared in the principal plane (front face) and rear face of this substrate body 4, and a through hole 7 which penetrates said substrate body 4. Said substrate body 4 is formed with the so-called GARAEOPO substrate which infiltrated epoxy resin into the glass fiber, and the ingredient (it has thermal resistance above 80 degrees C) of high thermal resistance into which BT resin was infiltrated while it has the thickness of 0.3mm. As for the wall of said through hole 7, plating is performed, and the wiring 5 and 6 on the rear face of front of the substrate body 4 is electrically connected by the conductor 8 by plating in the predetermined part. Moreover, said wiring 5 and 6 is formed by having pasted the front rear face of said substrate body 4, for example, etching copper foil with a thickness of about 15–35 micrometers into a desired pattern. Moreover, although illustration is not carried out to the front face of these wiring 5 and 6 so that connection by printing mentioned later may be made proper, partially or on the whole, plating processing by nickel and Au is performed. In addition, said wiring 6 serves as an external terminal, and, in the case of this example, forms the contact electrode terminal 21 for IC cards.

[0042] Next, as shown in drawing 2, the insulating glue line 9 is formed in the principal plane of the

substrate body 4 of screen-stencil. That is, the screen-stencil mask 15 with which the bore of the in general same configuration as said semiconductor chip 3 is established on the wiring substrate 2 is positioned in the location in which a semiconductor chip is carried. wiring (pad for connection) with which mask opening is formed in the printed circuit board — not starting — in addition — and it is desirable that it is larger than a semiconductor chip. Then, the thermosetting paste 16 for adhesion which has insulation is placed on said screen-stencil mask 15, a squeegee 17 is moved, the paste 16 for adhesion is imprinted on the wiring substrate 2, and the insulating paste layer 18 is formed.

[0043] On the other hand, fixed thickness polish and etching remove the rear-face side of a semiconductor chip 3, and about 5-30 micrometers in thickness are processed.

[0044] Next, as shown in drawing 3, the semiconductor chip 3 with a thickness of about 5-30 micrometers is carried on said insulating paste layer 18, and is pushed lightly. The insulating paste layer 18 which is under a semiconductor chip 3 by this is extruded slightly around a semiconductor chip 3, and it has been inhaled on the side face (end face) of a semiconductor chip 3. While this insulating paste layer 18 overflows and a part 19 plays the role which mitigates the level difference between the front face of the substrate body 4, and the top face of a semiconductor chip 3, the insulation of the end face of a semiconductor chip 3 will be performed. That the level difference of the semiconductor chip circumference becomes loose, generating of the defect of the conductor layer in a subsequent process will be improved remarkably.

[0045] Next the wiring substrate 2 in which the semiconductor chip 3 was carried is heated, the insulating paste layer 18 will be hardened, and will turn into the insulating glue line 9, and a semiconductor chip 3 will be fixed to the substrate body 4.

[0046] Next, in order to make more reliable the insulation to the end face of the insulator semiconductor chip 3, and flattening of a level difference, as shown in drawing 4 and drawing 6, the edge of wiring 5 is covered from the edge of a semiconductor chip 3 at least, and the insulator 11 with a thickness of about ten micrometers is formed from several micrometers in thickness by said same screen-stencil and hardening processing. That is, after printing an insulating paste to a predetermined pattern by screen-stencil, with heating, an insulating paste is stiffened and an insulator 11 is formed. an insulating paste — the thermal resistance after hardening — excelling (it having thermal resistance also in 80 degrees C or more) — what has resiliency is chosen. A resin system paste is used as what has such a property.

[0047] Next, as shown in drawing 5 and drawing 6, the conductor layer 12 which connects electrically the electrode 10 of a semiconductor chip 3 and the wiring 5 of the wiring substrate 2 is formed in said this appearance by screen printing. That is, a screen-stencil mask with opening for connecting electrically the wiring 5 of said wiring substrate 2 and the electrode 10 of a semiconductor chip 3 repeats printing to the wiring substrate 2, and a conductive paste is printed. A conductive paste also has resiliency while it scatters the silver of the shape of a flake with a magnitude of 1 micrometer - 5 micrometers by 70Wt(s)% - 80Wt% into the thermosetting resin which blended the curing agent with epoxy resin and has the thermal resistance after hardening (it has thermal resistance also in 80 degrees C or more). Of hardening processing, the conductor layer 12 which connects wiring 5 with an electrode 10 electrically is formed. This conductor layer 12 serves as thickness of several micrometers to about ten micrometers.

[0048] The semiconductor device 1 as shown in drawing 1 with the above procedure is manufactured. According to the manufacture approach of the semiconductor device of this example, the following hardening is done so.

[0049] (1) Since the connection between carrying a thin semiconductor chip in a wiring substrate, and the electrode of a semiconductor chip and wiring is based on the conductor layer by print processes according to the manufacture approach of the semiconductor device of this example, the semiconductor device of thin structure can be manufactured.

[0050] (2) Since crush an insulating paste in the formation phase of the insulating glue line which fixes a semiconductor chip, an insulating paste is made to protrude into the perimeter of a semiconductor chip and the level difference of a semiconductor chip and a wiring substrate is mitigated, before forming a conductor layer, in case a conductor layer is formed by print processes according to the manufacture

approach of the semiconductor device of this example, a printing blur stops occurring, the conductor layer of predetermined thickness can be formed, and the dependability of electrical installation becomes high.

[0051] (3) According to the manufacture approach of the semiconductor device of this example, since a printing blur is lost as mentioned above, the manufacture yield becomes high and can also attain the manufacture cost reduction of a semiconductor device.

[0052] (4) According to the manufacture approach of the semiconductor device of this example, since a wiring substrate, an insulator, and a conductor layer are formed with a heat-resistant ingredient, they can manufacture the semiconductor device excellent in thermal resistance.

[0053] (5) According to the manufacture approach of the semiconductor device of this example, since a wiring substrate, an insulator, and a conductor layer are formed with a flexible ingredient, they can manufacture the semiconductor device which was excellent to the mechanical shock.

[0054] The semiconductor device 1 of this example is built into IC card 20 as shown in drawing 7 and drawing 8 R> 8. That is, a semiconductor device 1 is fixed to the hollow 25 of the card base material 23 which becomes 0.76mm in thickness of IC card 20 by the card base material 23 with adhesives 24 with HAME ** rare **. The wiring 6 of a semiconductor device 1 serves as an external terminal, and forms the contact electrode terminal 21. In the IC card of this example, since HAME ** rare ***** is thin-shape-ized, a HAME **** hollow can be made shallow for a semiconductor device, the mechanical strength of a card base material improves, and the reinforcement to external force, such as bending of a semiconductor chip, improves by leaps and bounds. Therefore, according to this invention, the reinforcement of an IC card can be attained.

[0055] It cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned example, and does not deviate from the summary although invention made by this invention person above was concretely explained based on the example, for example, you may make it have formed the insulator for the end face of a semiconductor chip in the wrap sake in the case of said example, but form an insulator in a part for the edge surface part of a semiconductor chip beforehand instead of forming an insulator. Moreover, as a conductor layer which connects the electrode of a semiconductor chip, and wiring, the conductor layer of a thin film may be formed by the approaches, for example, the vacuum deposition method, and sputtering other than print processes. Moreover, film-like the insulation sheet and electric conduction sheet by which Puri shaping was carried out may be stuck and set.

[0056] Although the above explanation explained the case where invention mainly made by this invention person was applied to the IC card manufacturing technology which is a field of the invention used as the background, it is especially effective, when it is not limited to it, the semiconductor chip and passive element of loading to the substrate of electronic parts, such as resistance and a capacitor, and a large number like a hybrid IC are put in block and it connects. This invention is applicable to the electronic instrument which incorporates a semiconductor device (module) at least.

[0057]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly. According to this invention, the semiconductor device of a super-thin shape can be offered.

[0058] According to this invention, since thin shape-ization of the semiconductor device incorporated can be attained, the improvement in a mechanical strength of the card base material of the HAME lump part of a semiconductor device can be attained, and the reinforcement to external force, such as bending of a semiconductor chip, can offer the IC card excellent also in the dependability which can improve by leaps and bounds.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the typical sectional view showing the outline of the semiconductor device by one example of this invention.

[Drawing 2] It is the mimetic diagram showing the junction stratification condition in the manufacture approach of the semiconductor device by this example.

[Drawing 3] It is the typical sectional view showing the loading condition of the semiconductor chip in the manufacture approach of the semiconductor device by this example.

[Drawing 4] It is the typical sectional view showing the condition of having formed the insulator in the manufacture approach of the semiconductor device by this example.

[Drawing 5] It is the typical sectional view showing the condition of having formed the conductor layer in the manufacture approach of the semiconductor device by this example.

[Drawing 6] It is the typical top view showing the condition of having formed the insulator and the conductor layer in the manufacture approach of the semiconductor device by this example.

[Drawing 7] It is the typical sectional view showing the important section of the IC card by this example.

[Drawing 8] It is the top view showing the IC card by this example.

[Description of Notations]

1 — a semiconductor device, 2 — wiring substrate, 3 — semiconductor chip, and 4 — a substrate body, 5, 6 — wiring, 7 — through hole, and 8 — a conductor, 9 — insulation glue line, 10 — electrodes, and 11 — an insulator, 12 — conductor layer, 15 — screen-stencil mask, and 16 — the paste for adhesion, 17 — squeegee, 18 — insulation paste layer, and 19 — overflowing a part, 20 — IC card, 21 — contact electrode terminal, and 23 — a card base material, 24 — adhesives, and 25 — hollow.

[Translation done.]

(19)日本国特許庁 (JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平9-51020

(43)公開日 平成9年(1997)2月18日

(51)Int.Cl.⁶

H 01 L 21/60

G 06 K 19/077

識別記号

3 2 1

府内整理番号

F I

H 01 L 21/60

G 06 K 19/00

技術表示箇所

3 2 1 E

K

(21)出願番号 特願平7-201986

(22)出願日 平成7年(1995)8月8日

審査請求 未請求 請求項の数7 OL (全8頁)

(71)出願人 000005108

株式会社日立製作所

東京都千代田区神田駿河台四丁目6番地

(72)発明者 遠藤 恒雄

東京都小平市上水本町5丁目20番1号 株式会社日立製作所半導体事業部内

(74)代理人 弁理士 秋田 収喜

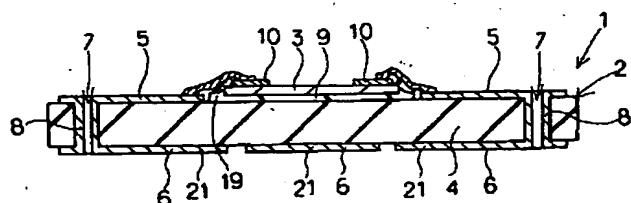
(54)【発明の名称】 半導体装置およびその製造方法ならびにICカード

(57)【要約】 (修正有)

【課題】 薄型化が達成できる半導体装置の提供。

【解決手段】 外部端子21を裏面に有する配線基板4と、配線基板の正面に固定された半導体チップ3と、半導体チップの電極10と配線基板4の配線5, 6とを電気的に接続する接続手段とを有する半導体装置であつて、少なくとも半導体チップ3の周縁から端面に及ぶ導電部分を覆う絶縁体と、半導体チップの電極10と配線基板の配線を電気的に接続する導体層とを有する。半導体チップは5~30μm前後の厚さとなっている。

図1



(2)

I

【特許請求の範囲】

【請求項 1】 外部端子を裏面に有する配線基板と、前記配線基板の正面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置であって、少なくとも前記半導体チップの周縁から端面に及ぶ導電部分を覆う絶縁体と、前記半導体チップの電極と配線基板の配線を電気的に接続する導体層とを有することを特徴とする半導体装置。

【請求項 2】 前記半導体チップは5～30μm前後の厚さとなっていることを特徴とする請求項1記載の半導体装置。

【請求項 3】 前記配線基板、絶縁体および導体層は耐熱性材料によって形成されていることを特徴とする請求項1記載の半導体装置。

【請求項 4】 前記配線基板、絶縁体および導体層は柔軟性を有する樹脂系材料で形成されていることを特徴とする請求項1記載の半導体装置。

【請求項 5】 裏面に外部端子を有する配線基板と、前記配線基板の正面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置の製造方法であって、半導体チップの裏面を除去して5～30μm前後の厚さに形成する工程と、前記配線基板の正面に絶縁性接着層を介して半導体チップを固定する工程と、前記半導体チップの縁から端面に亘る露出する導電部分を絶縁体で覆う工程と、印刷法によって前記半導体チップの電極と配線基板の配線を導体層で電気的に接続する工程とを有することを特徴とする半導体装置の製造方法。

【請求項 6】 前記配線基板に絶縁性接着層を介して半導体チップを固定する際、絶縁性接着層を配線基板に印刷した後、前記絶縁性接着層上に半導体チップを載置するとともに半導体チップを押さえ付けて前記絶縁性接着層を半導体チップの縁から外に食み出させることを特徴とする請求項5記載の半導体装置の製造方法。

【請求項 7】 カード基材の窪みに露出する外部端子を有する半導体装置を接着剤を介して組み込んでなるICカードであって、前記半導体装置は外部端子を裏面に有する配線基板と、前記配線基板の正面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置からなるとともに、少なくとも前記半導体チップの周縁から端面に及ぶ導電部分を覆う絶縁体と、前記半導体チップの電極と配線基板の配線を電気的に接続する導体層とを有し、かつ前記半導体チップは数十μmの厚さとなっていることを特徴とするICカード。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、半導体装置およびその製造方法ならびにICカードに関し、特に、薄型半導体

2

装置の製造に適用して有効な技術に関する。

【0002】

【従来の技術】 ICカードの一つの構造として、日経BP社発行「日経マイクロデバイス」1988年3月号、同年3月1日発行、P56～P62に記載されているように、LSIチップをトランスファ成形したモジュールを厚さ0.76mmのカードにハメ込む構造が知られている。前記モジュール(半導体装置)は、ガラス・エポキシ樹脂からなる配線基板の一面にCOB(chip on board)によって半導体チップを実装した後、半導体チップの電極と配線基板の配線とをワイヤボンディングによって電気的に接続するとともに、半導体チップ、ワイヤ等をトランスファ成形することによって製造される。また、前記配線基板の裏面には外部端子となる接触電極端子が設けられている。この接触電極端子は、前記配線基板に設けられたスルーホールに充填された導体によって配線基板の正面の配線に電気的に接続されている。

【0003】 一方、工業調査会発行「最新ハイブリッド実装技術」1988年5月15日発行、P26～P27、P38～P39には、生産性や高密度化を達成するために、ボンディングワイヤの代わりに接続用導電性ペーストを使用したICカード用のPWC(Printed Wiring Connection)や、ハイブリットICの事例が記載されている。

【0004】 前者のPWCによる組立は、ポリカーボネートシートに開口した部分にLSIチップを挿入した後埋め込み、その後、ポリカーボネートシートの表面およびLSIチップ上の埋め込み部分に亘って印刷によって印刷接続配線を形成するとともに、上下面をポリカーボネートフィルムで覆うようになっている。

【0005】 また、後者のハイブリッドICの場合は、A1基板内にICチップをエポキシ樹脂で埋め込み、感光性の導体ペースト、絶縁ペーストを用いて配線した構造となっている。

【0006】 なお、これらの構造では、半導体チップを配線基板に埋め込む構造となるとともに、配線基板の表面と半導体チップの上に形成された電極とは略同一平面上にある構造となっている。したがって、接続用の導電性パターン(導体層)の形成に際しては、半導体チップの電極と配線基板の配線との間に段差が発生しない状態にある。

【0007】

【発明が解決しようとする課題】 COB構造の半導体装置(モジュール)では、半導体チップの電極と配線基板の配線とはワイヤボンディングによって接続される構造となるため、ワイヤループ高さ分だけ半導体装置が厚くなってしまい、ICカードにハメ込む(埋め込む)構造では、ハメ込むための窪みが深くなり、ICカードの窪み部分の機械的強度が低くなる。

【0008】 一方、配線基板に設けた穴部分に半導体チップを埋め込む構造では、配線基板の配線の表面と半導

(3)

3

体チップの電極とを同一の面になるようにして段差を無くし、印刷法で半導体チップの電極と配線とを電気的に接続する方法を採用している。しかし、半導体チップの埋め込みには手間がかかる事、又不良品が発生した場合には交換（リペア）が大変難しい等の問題があり、安価に作る事が難しい。安価に作る為には、半導体チップを配線基板の上に直接搭載することが必要である。

【0009】半導体チップの電極と配線を印刷法による導体層で接続する構造は、導体層が高くならないことから、半導体装置（モジュール）の薄型化を達成できる。

【0010】そこで、本発明は、配線基板の主面に半導体チップを搭載するとともに、印刷法によって半導体チップの電極と配線とを接続することを考えた。しかし、従来の半導体チップ、すなわち、LSIチップは、その厚さが $200\mu\text{m} \sim 500\mu\text{m}$ となるため、半導体チップの電極と配線間に段差が生じ、導電性ペーストを印刷した時に、前記段差部で印刷かすれが発生しやすく、接続が不充分となってしまうことが分かった。

【0011】本発明の目的は、薄型化が達成できる半導体装置およびその製造方法を提供することにある。

【0012】本発明の他の目的は、カード基材の機械的強度向上が達成できるICカードを提供することにある。

【0013】本発明の前記ならびにそのほかの目的と新規な特徴は、本明細書の記述および添付図面からあきらかになるであろう。

【0014】

【課題を解決するための手段】本願において開示される発明のうち代表的なものの概要を説明すれば、次の通りである。すなわち、本発明の半導体装置は、外部端子を裏面に有する配線基板と、前記配線基板の主面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置であって、少なくとも前記半導体チップの周縁から端面に及ぶ導電部分を覆う絶縁体と、前記半導体チップの電極と配線基板の配線を電気的に接続する導体層とを有する構造となっている。前記半導体チップは $5 \sim 30\mu\text{m}$ 前後の厚さとなっている。また、前記配線基板、絶縁体および導体層は耐熱性材料によって形成されているとともに、柔軟性を有する樹脂系材料で形成されている。

【0015】本発明の半導体装置の製造方法は、裏面に外部端子を有する配線基板と、前記配線基板の主面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置の製造方法であって、半導体チップの裏面を除去して $5 \sim 30\mu\text{m}$ 前後の厚さに形成する工程と、前記配線基板の主面に絶縁性接着層を介して半導体チップを固定する工程と、前記半導体チップの縁から端面に亘る露出する導電部分を絶縁体で覆う工程と、印刷法によ

って前記半導体チップの電極と配線基板の配線を導体層で電気的に接続する工程とからなっている。また、前記配線基板に絶縁性接着層を介して半導体チップを固定する際、絶縁性接着層を配線基板に印刷した後、前記絶縁性接着層上に半導体チップを載置するとともに半導体チップを押さえ付けて前記絶縁性接着層を半導体チップの縁から外に食み出させ、その後導体層の印刷を行う。

【0016】本発明のICカードは、カード基材の窪みに露出する外部端子を有する半導体装置を接着剤を介して組み込んでなるICカードであって、前記半導体装置は外部端子を裏面に有する配線基板と、前記配線基板の主面に固定された半導体チップと、前記半導体チップの電極と配線基板の配線とを電気的に接続する接続手段とを有する半導体装置からなるとともに、少なくとも前記半導体チップの周縁から端面に及ぶ導電部分を覆う絶縁体と、前記半導体チップの電極と配線基板の配線を電気的に接続する導体層とを有し、かつ前記半導体チップは $5 \sim 30\mu\text{m}$ 前後の厚さとなっている。

【0017】

【作用】前記した手段によれば、本発明の半導体装置は、数十 μm と薄くなった半導体チップを配線基板に搭載するとともに、印刷による導体層によって半導体チップの電極と配線基板の配線とが電気的に接続されていることから、半導体装置の薄型化が達成できる。

【0018】本発明の半導体装置は、半導体チップの電極と配線基板の配線とは印刷による導体層によって電気的に接続されているが、この導体層の下には前記半導体チップの周縁から端面の露出する導電部分を覆う絶縁体が設けられているため、半導体チップの隣合う電極部分間の短絡が発生しない。

【0019】本発明の半導体装置は、配線基板、絶縁体および導体層は耐熱性材料によって形成されていることから半導体装置の耐熱性が良好となる。

【0020】本発明の半導体装置は、配線基板、絶縁体および導体層は、柔軟性を有する樹脂系材料で形成されていることから、半導体チップの電極と配線との電気的接続の信頼性が高くなる。

【0021】本発明の半導体装置の製造方法によれば、半導体チップを薄くした後配線基板に実装することと、半導体チップの電極と配線基板の配線を印刷法による導体層によって接続することから、薄い半導体装置を製造することができる。

【0022】また、本発明の半導体装置の製造方法によれば、半導体チップの電極と配線基板の配線を印刷法によって電気的に接続する前に、半導体チップの周縁および端面の導電部分は絶縁体で被覆することから、半導体チップの隣合う電極部分間の短絡が発生しなくなる。

【0023】また、前記配線基板に半導体チップを固定する際、絶縁性接着層を配線基板に印刷した後、前記絶縁性接着層上に半導体チップを載置するとともに半導体

(4)

5

チップを押さえ付けて前記絶縁性接着層を半導体チップの縁から外に食み出させている。したがって、その後の導体層の印刷においては、半導体チップと配線との間に絶縁性接着層が延在するため、半導体チップと配線基板との間の段差が低減され、半導体チップの電極と配線を接続する導体層のかすれ等が発生しなくなり、安定した電気的接続が可能となる。

【0024】本発明のICカードは、ハメ込まれる半導体装置が薄型化されていることから、半導体装置をハメ込む窪みを浅くすることができ、カード基材の機械的強度が向上する。

【0025】

【実施例】以下図面を参照して本発明の一実施例について説明する。図1は本発明の一実施例による半導体装置の概要を示す模式的断面図である。図2～図6は本実施例の半導体装置の製造方法における各工程での半導体装置の要部を示す図であって、図2は接合層形成状態を示す模式図、図3は半導体チップの搭載状態を示す模式的断面図、図4は絶縁体を形成した状態を示す模式的断面図、図5は導体層を形成した状態を示す模式的断面図、図6は絶縁体および導体層を形成した状態を示す模式的平面図である。図7は本実施例によるICカードの要部を示す模式的断面図、図8は同じくICカードを示す平面図である。

【0026】本実施例の半導体装置（モジュール）1は、図7および図8に示すICカード20にハメ込まれるICカード用モジュールであり、図1に示すように、配線基板2と、この配線基板2の正面に搭載された半導体チップ3とを有する構造となっている。

【0027】配線基板2は、基板本体4と、この基板本体4の正面（表面）および裏面に設けられた配線5、6と、前記基板本体4を貫通するスルーホール7とからなるプリント基板となっている。前記基板本体4は、ガラス繊維にエポキシレジンを含浸させた所謂ガラエポ基板や、BTレジンを含浸させた高耐熱性の材料からなっている。この基板本体4は80°C以上においても耐熱性を有している。また、前記基板本体4は厚さ0.3mm程度となっている。前記配線5、6は、前記基板本体4の表裏面に接着した、たとえば35μm程度の厚さの銅箔を所望のパターンにエッチングすることによって形成される。また、この配線5、6の表面には、後述する印刷による接続が適正に実施されるように、図示はしないが、NiおよびAuによるめっき処理が部分的または全体的に施されている。

【0028】また、前記スルーホール7は基板本体4を貫通するようにドリル加工することによって形成されている。このスルーホール7の内壁面には銅メッキが施されている。この銅メッキによって形成された導体8によって、基板本体4の表裏面の所定の配線5、6は電気的に接続される。

6

【0029】本実施例の半導体装置1の裏面の配線6は、図8に示すように、ICカード20の外部端子となる接触電極端子21を構成する。

【0030】また、配線基板2の正面には絶縁性接着層9を介して半導体チップ3が固定されている。半導体チップ3はアクティブ領域が設けられない裏面側がエッチング等によって一定の厚さ除去され、たとえば、5～30μm程度の厚さとなっている。これは半導体チップ3の表面に設けられた電極10と、配線基板2の配線5の高さとの段差が大きくならないようにするためである。

【0031】また、図6に示すように、前記半導体チップ3の少なくとも周縁から端面に及ぶ導電部分を覆うように、柔軟性を有しあつ耐熱性を有する材料で形成された絶縁体11が設けられている。前記絶縁体11は80°C以上で耐熱性がある樹脂系材料で形成されている。また、前記絶縁体11上には柔軟性を有しあつ耐熱性を有する材料で形成された導体層12が設けられている。導体層12は前記半導体チップ3の電極10と配線基板2の配線5を電気的に接続する。前記導体層12は80°C以上で耐熱性がある樹脂系材料で形成されている。前記絶縁体11および導体層12はスクリーン印刷法によって形成される。

【0032】なお、前記半導体チップ3の周囲には、半導体チップ3を基板本体4に接続する絶縁性接着層9の食み出し部分が存在するため、半導体チップ3の縁から配線5の縁に亘る部分に設けられた絶縁体11は、前記食み出し部分が半導体チップ3と基板本体4との間の段差を軽減することになるため、平坦化されて形成される。したがって、この平坦化された絶縁体11上に設けられる導体層12も平坦化され、部分的に薄くなるなど電気的接続に不都合となるようなかすれば生じなくなる。

【0033】また、図6に示すように、前記絶縁体11は半導体チップ3の縁から配線5の先端部分に亘って設けられるとともに、前記絶縁体11上に導体層12が設けられるため、隣接する電極10間の短絡が防止される。

【0034】本実施例の半導体装置1は、半導体チップ3が5～30μmと薄く形成されていることと、半導体チップ3の電極10と配線基板2の配線5とを接続する導体層12が絶縁体11を介して配線基板2上を這うように形成されていることから、ワイヤボンディング構造に比較して大幅に薄くなる。すなわち、従来のワイヤボンディング構造の場合、配線基板2上には200～500μmの厚さの半導体チップが載置されるとともに、この半導体チップの電極にワイヤループ高さが150μm程度となるワイヤが接続される。また、前記ワイヤおよび半導体チップはトランスマウルドによって形成されるパッケージによって被覆される。したがって、配線基板の表面からパッケージ上面までの高さは少なくとも

(5)

7

500 μm 程度と高くなる。これに対して、本実施例の半導体装置の場合、半導体チップや導体層をパッケージで被覆しないこともあり、配線基板の表面から導体層の上面までの高さは15～40 μm 程度と1桁以上も低くなり、半導体装置1の薄型化が達成できる。このため、本実施例の半導体装置1を、図7に示すように、絶縁性の接着剤24を介して、カード基材23に設けられた窪み25にハメ込む場合、前記窪み25を従来よりも百数十 μm 程度浅くできることになり、窪み25が設けられるカード基材23部分の機械的強度が向上する。

【0035】本実施例の半導体装置は以下の効果を奏する。

【0036】(1) 本実施例の半導体装置は、基板本体の正面に5～30 μm 前後の厚さの半導体チップを搭載する構造となることから、半導体装置の薄型化が達成される。

【0037】(2) 本実施例の半導体装置は、半導体チップの電極と、配線基板の配線との接続は、印刷法によって形成される導体層によって接続されるため、半導体装置の薄型化が達成される。

【0038】(3) 本実施例の半導体装置においては、半導体チップの電極と配線基板の配線とを接続する導体層および導体層の下地となる絶縁体ならびに配線基板は、柔軟性を有する樹脂系材料で形成されていることから、半導体チップの電極と配線基板の配線との電気的接続の信頼性が高くなる。

【0039】(4) 本実施例の半導体装置においては、半導体チップの電極と配線基板の配線とを接続する導体層および導体層の下地となる絶縁体ならびに配線基板は、耐熱性材料によって形成されていることから、半導体装置の耐熱性が向上する。

【0040】(5) 本実施例の半導体装置においては、半導体チップの電極と配線基板の配線とを接続する導体層の下には絶縁体が設けられていることから、導体層間の短絡防止効果が高くなり、半導体装置の電極間の短絡が発生しなくなる。

【0041】つぎに、本実施例の半導体装置1の製造方法について、図2～図6を用いて説明する。図2に示すように、最初に配線基板2が用意される。この配線基板2は、基板本体4と、この基板本体4の正面(表面)および裏面に設けられた配線5、6と、前記基板本体4を貫通するスルーホール7とからなるプリント基板となっている。前記基板本体4は、たとえば、0.3 mmの厚さを有するとともに、ガラス繊維にエポキシレジンを含浸させた所謂ガラエポ基板や、BTレジンを含浸させた高耐熱性の材料(80°C以上で耐熱性を有する)で形成されている。前記スルーホール7の内壁はメッキが施され、メッキによる導体8によって基板本体4の表裏面の配線5、6は所定箇所で電気的に接続されている。また、前記配線5、6は、前記基板本体4の表裏面に接着

(5)

8

した、たとえば15～35 μm 程度の厚さの銅箔を所望のパターンにエッチングすることによって形成される。また、この配線5、6の表面には、後述する印刷による接続が適正に実施されるように、図示はしないが、NiおよびAuによるめっき処理が部分的または全体的に施されている。なお、前記配線6は外部端子となり、本実施例の場合にはICカード用の接触電極端子21を形成している。

【0042】つぎに、図2に示すように、スクリーン印刷によって基板本体4の正面には、絶縁性接着層9が形成される。すなわち、配線基板2上には、前記半導体チップ3と概ね同一な形状の透孔が開設されているスクリーン印刷マスク15が、半導体チップが搭載される位置に位置決めされる。マスク開口部はプリント基板に形成されている配線(接続用パッド)に掛からず、なおかつ半導体チップより大きいことが望ましい。その後、前記スクリーン印刷マスク15上に絶縁性を有する熱硬化性の接着用ペースト16を置き、スキージ17を移動させて接着用ペースト16を配線基板2上に転写して絶縁ペースト層18を形成する。

【0043】一方、半導体チップ3の裏面側を一定厚さ研磨やエッチングによって除去して、厚さ5～30 μm 程度に加工しておく。

【0044】つぎに、図3に示すように、厚さ5～30 μm 程度の半導体チップ3を前記絶縁ペースト層18上に載せ軽く押し付ける。これにより半導体チップ3の下にある絶縁ペースト層18が、半導体チップ3の周辺に僅かに押し出され、半導体チップ3の側面(端面)に吸い上がる。この絶縁ペースト層18の食み出し部分19は、基板本体4の表面と半導体チップ3の上面との間の段差を軽減する役割を果たすとともに、半導体チップ3の端面の絶縁が行われることになる。半導体チップ周辺の段差が緩やかとなることは、その後の工程での導体層の欠陥の発生が著しく改善されることになる。

【0045】つぎに、半導体チップ3の搭載された配線基板2は加熱され、絶縁ペースト層18は硬化して絶縁性接着層9となり、半導体チップ3を基板本体4に固定することになる。

【0046】つぎに、絶縁体半導体チップ3の端面への絶縁性と、段差の平坦化をより確実にするために、図4および図6に示すように、少なくとも半導体チップ3の縁から配線5の縁に亘って前記同様のスクリーン印刷および硬化処理によって厚さ数 μm から十数 μm の厚さの絶縁体11を形成する。すなわち、スクリーン印刷によって、所定パターンに絶縁性ペーストを印刷した後、加熱によって絶縁性ペーストを硬化させて絶縁体11を形成する。絶縁性ペーストは、硬化後耐熱性に優れる(80°C以上においても耐熱性を有する)とともに、弾力性を有するものが選択される。このような特性を有するものとして、樹脂系ペーストが使用される。

(6)

9

【0047】つぎに、図5および図6に示すように、半導体チップ3の電極10と、配線基板2の配線5とを電気的に接続する導体層12が、前記同様にスクリーン印刷法によって形成される。すなわち、印刷は前記配線基板2の配線5と半導体チップ3の電極10を電気的に接続するための開口部を持ったスクリーン印刷マスクが、配線基板2に重ねられ、導電性ペーストが印刷される。導電性ペーストは、エポキシレジンと硬化剤を配合した熱硬化性レジンの中に、 $1\text{ }\mu\text{m} \sim 5\text{ }\mu\text{m}$ の大きさのフレーク状の銀を $7.0\text{ Wt\%} \sim 8.0\text{ Wt\%}$ 分散させたものであり、硬化後耐熱性（ 80°C 以上においても耐熱性を有する）を有するとともに、弾力性をも有する。硬化処理によって、電極10と配線5を電気的に接続する導体層12が形成される。この導体層12は数 μm から十数 μm の厚さとなる。

【0048】以上の手順によって図1に示すような半導体装置1が製造される。本実施例の半導体装置の製造方法によれば以下の硬化を奏する。

【0049】（1）本実施例の半導体装置の製造方法によれば、薄い半導体チップを配線基板に搭載することと、半導体チップの電極と配線との接続は印刷法による導体層によるため、薄型構造の半導体装置を製造できることになる。

【0050】（2）本実施例の半導体装置の製造方法によれば、導体層を形成する前に、半導体チップを固定する絶縁性接着層の形成段階で絶縁性ペーストを押し潰して半導体チップの周囲に絶縁性ペーストを食み出させて半導体チップと配線基板との段差の軽減を行うことから、導体層を印刷法によって形成する際、印刷かすれが発生しなくなり、所定の厚さの導体層を形成することができ、電気的接続の信頼性が高くなる。

【0051】（3）本実施例の半導体装置の製造方法によれば、前記のように印刷かすれがなくなることから製造歩留りが高くなり、半導体装置の製造コスト低減も達成できる。

【0052】（4）本実施例の半導体装置の製造方法によれば、配線基板、絶縁体、導体層は耐熱性材料によって形成されることから、耐熱性に優れた半導体装置を製造することができる。

【0053】（5）本実施例の半導体装置の製造方法によれば、配線基板、絶縁体、導体層は柔軟な材料によって形成されることから、機械的衝撃に対して優れた半導体装置を製造することができる。

【0054】本実施例の半導体装置1は、図7および図8に示すように、ICカード20に組み込まれる。すなわち、半導体装置1は、ICカード20の厚さ0.76mmとなるカード基材23の窪み25にハメ込まれるとともに、接着剤24によってカード基材23に固定される。半導体装置1の配線6は、外部端子となり、接触電極端子21を形成する。本実施例のICカードにおいて

(6)

10

は、ハメ込まれる半導体装置が薄型化されていることから、半導体装置をハメ込む窪みを浅くすることができ、カード基材の機械的強度が向上し、半導体チップの折り曲げ等の外力に対する強度が飛躍的に向上する。したがって、本発明によればICカードの長寿命化が達成できる。

【0055】以上本発明者によってなされた発明を実施例に基づき具体的に説明したが、本発明は上記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない、たとえば、前記実施例の場合は半導体チップの端面を覆うために絶縁体を設けているが、絶縁体を設ける代わりに、半導体チップの端面部分に絶縁体を予め設けるようにしてもよい。また、半導体チップの電極と配線とを接続する導体層としては、印刷法以外の方法、たとえば、真空蒸着法やスパッタリングによって薄膜の導体層を形成してもよい。また、プリ成形されたフィルム状の絶縁シートや導電シートを貼りあわせてもよい。

【0056】以上の説明では主として本発明者によってなされた発明をその背景となつた利用分野であるICカード製造技術に適用した場合について説明したが、それに限定されるものではなく、抵抗、コンデンサ等の電子部品の基板への搭載や、ハイブリッドICの様な多数の半導体チップや受動素子を一括して接続する場合に、特に有効である。本発明は少なくとも半導体装置（モジュール）を組み込む電子装置には適用できる。

【0057】

【発明の効果】本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば、下記のとおりである。本発明によれば、超薄型の半導体装置を提供することができる。

【0058】本発明によれば、組み込まれる半導体装置の薄型化が達成できることから、半導体装置のハメ込み部分のカード基材の機械的強度向上が達成でき、半導体チップの折り曲げ等の外力に対する強度が飛躍的に向上できる信頼性にも優れたICカードを提供できる。

【図面の簡単な説明】

【図1】本発明の一実施例による半導体装置の概要を示す模式的断面図である。

【図2】本実施例による半導体装置の製造方法における接合層形成状態を示す模式図である。

【図3】本実施例による半導体装置の製造方法における半導体チップの搭載状態を示す模式的断面図である。

【図4】本実施例による半導体装置の製造方法において絶縁体を形成した状態を示す模式的断面図である。

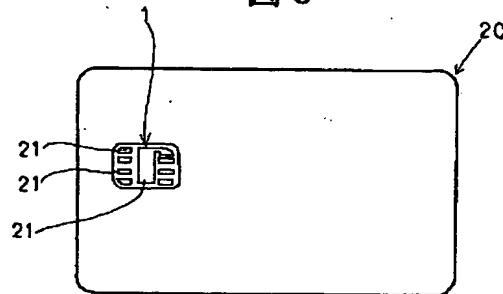
【図5】本実施例による半導体装置の製造方法において導体層を形成した状態を示す模式的断面図である。

【図6】本実施例による半導体装置の製造方法において絶縁体および導体層を形成した状態を示す模式的平面図である。

(8)

【図8】

図8



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.